Performance Evaluation of a Self-Biased Current Reference Source Using Uniformly Doped and Halo-Implanted Channel Transistors

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***Abstract*—This paper presents a performance comparison of a self-biased current reference source tolerant to supply voltage variations built with uniformly doped and halo-implanted channel transistors. The proposed topology was designed in a 130 nm CMOS process to provide a current reference of 30 μA under 3.3 V supply voltage. The results obtained proves a better performance of the uniformly doped transistors with a current reference's sensitivity to supply voltage of 0.7% and a temperature coefficient of 23.8 ppm/ºC, whilst the halo-implanted transistors has a current reference's sensitivity to supply voltage of 15.3% and a temperature coefficient of 66.8 ppm/ºC.**

***Index Terms*—current source, CMOS current reference source, halo-implanted CMOS transistor.**

I. Introduction

A current reference source is a fundamental building block in an integrated circuit design and must be able to supply an accurate current with a reduced current sensitivity with respect to temperature and voltage supply. Usually, a current reference source is load dependent, but it is possible to avoid this effect adding circuits that isolate the current reference from the load and maintain your performance [1].

In the design of current reference sources, there is an effort to make the current reference value independent from the supply voltage [2, 3]. A way to minimize the dependence of the current reference in relation to the supply voltage is to implement a circuit that the operating point is established by the current reference itself. This concept can be illustrated when a positive feedback loop requires the input current to be equal to the output current, characterizing a self-biased current reference source [4].

The uniformly doped transistors are the most advisable for analog operations. However, in this paper we introduce an implementation of the current reference using halo-implanted, used in digital circuit designs [5]. Due to doping variation along the channel, the halo-implanted have a fluctuation in the mobility of the carriers and in the threshold voltage, resulting in a low output impedance and a high mismatch [6]–[8].

In this paper, we introduce a self-biased current source using a 130 nm CMOS technology with a 3.3 V supply voltage and a 30 μA current. Furthermore, the objective of this work is compare the performance of the self-biased current using transistors with uniformly doped and halo-implanted channels. The results obtained shows a better performance of the uniformly doped transistors for having a current reference's sensitivity to supply voltage and a temperature coefficient lower than the halo-implanted transistors.

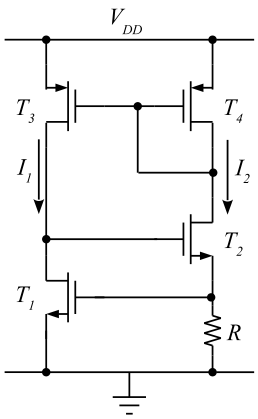


Fig. 1. Self-biased current reference source circuit.

The paper has the following structure. In Section II, grounds the self-biased current source threshold voltage based. In Section III, describes the circuit topology design. In Section IV the results obtained in the implementation of the circuit are discussed. Finally, in Section V, presents the conclusions and final considerations of this paper.

II. A self-biased current reference source based on the MOSFET threshold voltage

The circuit seen in Fig. 1 was based on the concept of positive feedback loop and represents a self-biased current source. The current source block consists on matched T_1 and T_2 MOS transistors and a resistor R that dictates the value of I_2, as

$$I_2 = \frac{V_{GS_1}}{R} \ , \tag{1}$$

which depends weakly on I_1, given by

$$I_1 = \mu_n C_{ox} \left(\frac{W}{L}\right)_1 (V_{GS_1} - V_{TH})^2 \ , \tag{2}$$

neglecting the body effect [1].

Manipulating (1) and (2) it can be derived expressions to V_{GS_1} and I_2 as

$$V_{GS_1} = \sqrt{\frac{2I_1L}{\mu_n C_{ox} W}} + V_{TH_1} \text{ and} \tag{3}$$

$$I_2 = \frac{\sqrt{\frac{2I_1L}{\mu_n C_{ox} W}}}{R} + \frac{V_{TH_1}}{R} \ . \tag{4}$$

Transistors T_3 and T_4 of Fig. 1 are configured as a current mirror thus I_2 is copied to I_1. Hence, I_1 current flows to T_1 creating a V_{GS_1} voltage determining I_2 current that flows through R. This relationship implements a positive feedback. Thus, the balance between I_1 and I_2, determined by V_{GS_1}, causes the circuit to self-biasing [4].

Therefore, equating I_1 and I_2 regarding V_{GS_1}, it is possible to obtain the current reference value I_Q as

$$I_Q = I_1 = I_2 = \frac{V_{TH_1}}{R} + \frac{1}{\beta_1 R^2} + \frac{1}{R}\sqrt{\frac{2V_{TH_1}}{\beta_1 R} + \frac{1}{\beta_1^2 R^2}} \ , \tag{5}$$

where $\beta_1 = \mu_n C_{ox} \left(W/L\right)_1$.

There are two operating points in which I_1 and I_2 are equal, when $I_1 = I_2 = 0$ and $I_1 = I_2 = I_Q$. When $I_1 = I_2 = 0$, the gain around the positive feedback is deliberately made greater than unity, causing I_1 and I_2 to intersect at a point away from the origin. The operating point away from the origin is the value of I_Q current reference, in which the gain of the positive feedback is small causing I_1 and I_2 stabilizing in the intended I_Q current reference value [1].

The circuit sensitivity $S_{V_{DD}}^{I_Q}$ is a relationship between the reference and supply voltage characterizing the performance of the current reference source allowing comparisons, then

$$S_{V_{DD}}^{I_Q} = \frac{V_{DD}}{I_Q}\frac{\partial I_Q}{\partial V_{DD}} \times 100 \ . \tag{6}$$

Despite the absence of a temperature compensation block, another performance indicator for the circuit in Fig. 1 is the variation of the current reference regarding the temperature. According to [4], the temperature coefficient is calculated by deriving the current equation to the temperature. Thus, the temperature coefficient of the circuit in Fig. 1 is

$$TC = \frac{1}{I_Q}\frac{\partial I_Q}{\partial T} = \frac{1}{V_{GS_1}}\frac{\partial V_{GS_1}}{\partial T} - \frac{1}{R}\frac{\partial R}{\partial T} \ . \tag{7}$$

III. Design of a current reference source in a 130 nm CMOS Process

The project and simulation were performed using the BSIM4v4 model for an GF 130 nm CMOS process (GF-8RF). All simulations were performed at room temperature (27 ºC).

In the simulation of the circuit seen in Fig. 1, a 3.3 V supply voltage was chosen. For a 30 μA current flows at a 30 kΩ resistance, is required a voltage of 0.9 V over R. Then, T_2 and T_4 has a voltage drop of, approximately, 1.2 V.

The resistor R was chosen with precision polysilicon, for having the smallest TC among those available in the GF 130 nm CMOS process, 1.70 ppm/ºC, although the purpose of the project is only the independence of the current reference regarding to the power supply variations.

A. Transistor sizing

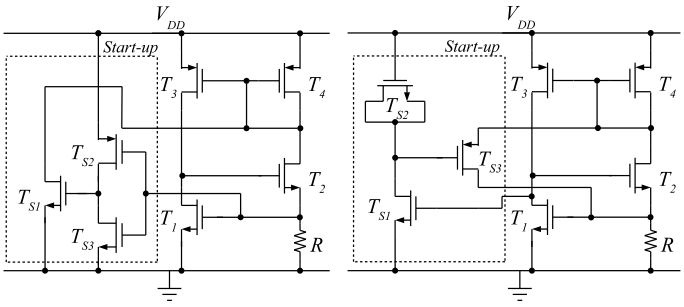
A transistor with a long channel is the most suitable for analog operations, as it is possible to neglect the effect of modulating the length of the channel. Therefore, we define that the channel length of the nMOS and pMOS transistors would be respectively $50L_{min}$ and $5L_{min}$, where L_{min} of the GF 130 nm CMOS process is equal to 500 nm for 3.3 V the uniformly doped transistor. We choose to maintain the same length for the halo-implanted transistor. although the width changes as $u_n C_{ox}$ and V_{TH} are different from uniformly doped, then for the same I_{DS} current, halo-implanted transistors needs to compensate in width. Table I contains the aspect ratios (W/L).

TABLE I
TRANSISTORS ASPECT RATIO

Transistors [μm/μm]	Uniformly Doped	Halo-Implanted
T_1 and T_2	36.5 / 25.0	5.4 / 25.0
T_3 and T_4	5.4 / 2.5	2.3 / 2.5

B. Start-up Circuit

A start-up circuit is used to ensure that the circuit reaches the condition of $I_1 = I_2 = I_Q$. Therefore, we implement from Fig. 2a and 2b, in order to compare the start-up time and the active area.



(a) CMOS Inverter (b) MOS Capacitor

Fig. 2. Self-Biasing Reference Source with a startup circuit.

The start-up circuit in Fig. 2a was based on [4] in which T_{S2} and T_{S3} form a CMOS inverter. The circuit in Fig. 2b was based on [9], an approach that does not consume static energy and is more tolerant to supply voltage variation. The circuit uses the T_{S2} transistor operating as a CMOS capacitor.

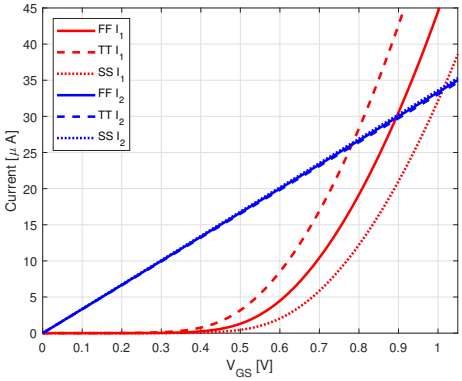
In both start-up circuit design, only halo-implanted transistors with minimal dimensions W/L equals to 160 nm/120 nm were used. The start-up circuit only ensure the reference circuit begins to operate and then stops interfering with the reference circuit operation.

IV. Results and Discussion

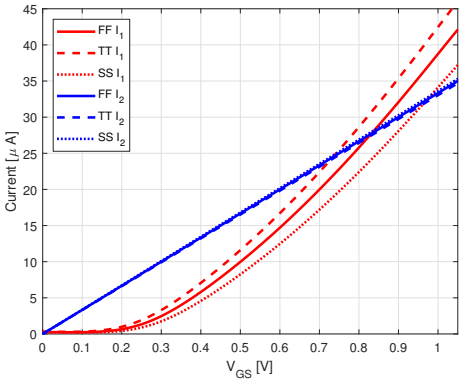
In order to obtain a behavioral estimation of this circuit related to fabrication process variations we perform corners and Monte Carlo simulations. The corners simulation were performed using FF, TT and SS models, i.e., process variations

for fast, typical and slow nMOS and pMOS transistors, respectively. From Fig. 3a, I_2 shows no relevant variation because, as seen in (1), it depends on resistance R value which is barely affected by the process variation. However, as seen in (2), I_1 depends on β which varies according to the manufacturing process. Thus, the current reference I_Q stabilizes in different values in FF and SS models. The values of I_Q found for FF, TT and SS models are, respectively, 25.8 μA, 30.0 μA and 34.2 μA.

The same corners simulation we perform for the circuit using halo-implanted transistors, the results are shown in Fig. 3b. The same variation impact of β in I_1 and the low variation of I_2 can be observed. In which causes the variation of the current reference I_Q because they are not able to maintain the intended biasing. The values of I_Q found for FF, TT and SS models in this circuit are, respectively, 24.3 μA, 27.7 μA and 33.0 μA.



(a) Uniformly Doped

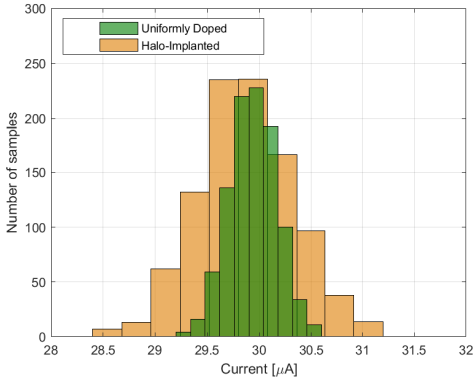


(b) Halo-Implanted

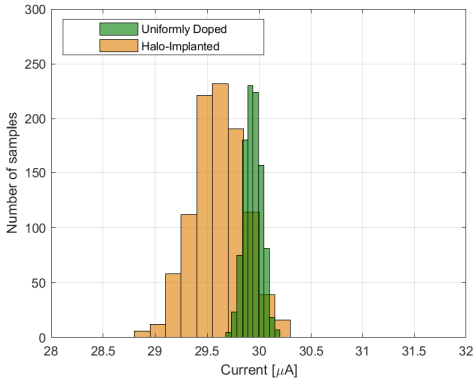
Fig. 3. Behavior of I_1 and I_2 to process corners.

The Monte Carlo simulation analyses the mismatch variations related to I_1 and I_2 using halo-implanted and uniformly doped transistors. Fig. 4 shows the results obtained in histograms of the I_1 and I_2 behavior for uniformly doped and halo-implanted transistors.

Analyzing the results obtained from the Monte Carlo simulation, the high mismatch characteristic of halo-implanted transistors can be noticed, because their standard deviation is higher compared to uniformly doped transistors, as 0.48% and 0.23% for the halo-implanted and uniformly doped, respectively. Fig. 4 also shows I_1 has a greater variation than I_2, because, as seen in corners simulation, I_1 is more dependent on the manufacturing process than I_2.



(a) Current I_1



(b) Current I_2

Fig. 4. Behavior of I_1 and I_2 in histograms using uniformly doped and halo-implanted transistors in a Monte Carlo simulation analysing mismatch variation (1000 runs).

It is possible to see in Fig. 5 the behavior of I_Q versus V_{DD} ranging from 3 V to 3.6 V. As shown, I_Q variation for the circuit built with halo-implanted is higher than the uniformly doped circuit. Applying (6), it can be found a sensitivity $S_{V_{DD}}^{I_Q}$ of 0.7% for uniformly doped transistors and 15.3% for halo-implanted transistors. This difference is due to halo-implanted not having a well-defined saturation current, thus making the current reference source circuit more susceptible to supply voltage variations.

Fig. 6 shows the curves of I_1 and I_2 related to the temperature variation, as shown the uniformly doped transistors is less susceptible to temperature variation than the circuit built with halo-implanted transistors. Additionally, the circuit with halo-implanted transistors presents a mismatch between I_1 and I_2 near the I_Q operating point. The sensitivity of the current reference source related to the temperature is given by (7). The TC values for the circuits built with uniformly doped and halo-implanted transistors are, respectively, 23.8 ppm/^{o}C and 66.8 ppm/^{o}C.

A ramp signal is apply to analyze the operation of the circuit when it turns on. We perform a transient simulation using a rise time of 10 μs. The startup time is measured when the circuits

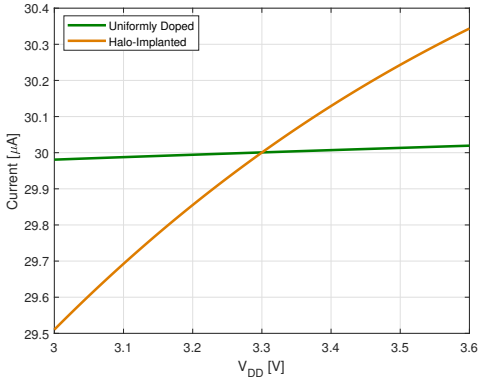


Fig. 5. Variation of $I_Q \times V_{DD}$ using doped uniformly and halo-implanted transistors.

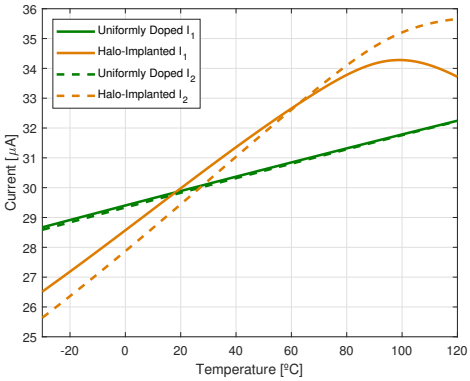
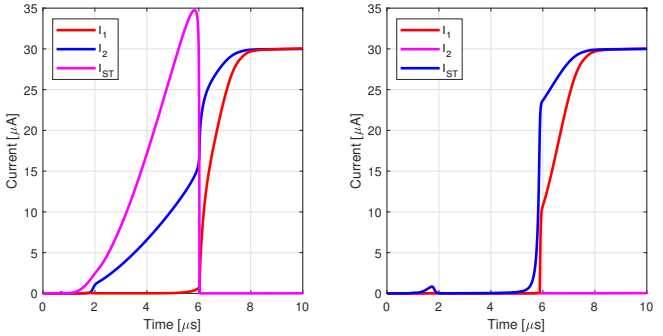


Fig. 6. Variation of I_1 and I_2 related to temperature using uniformly doped and halo-implanted.

starts to turn on to achieve 90% of the current reference value, i.e., 27 μA. Fig. 7a and 7b show the transient simulations obtained for the start-up circuits. It is possible to see that what differs in both circuits is the maximum current drained by the start-up circuit and the maximum current after achieve the current reference. The maximum current drained by the start-up circuit with the CMOS inverter is 34.75 μA, while the circuit start-up with the MOS capacitor is 0.04 μA. The maximum current after achieve the current reference of 30 μA by the start-up with MOS inverter and with MOS capacitor is, respectively, 0.01 μA and 0.03 μA. The startup time and active area are the same for both circuits, 6.66 μs and 7969 μm^2, respectively. The start-up circuit chosen to initialize the current reference source is the circuit start-up with MOS capacitor for having a low maximum current drained compared to the start-up with MOS inverter.

V. Conclusion

The purpose of this paper was to compare the performance of a current reference source tolerant to supply voltage variations built with uniformly doped and halo-implanted transistors. We designed a topology with a biasing established by it is own current reference, thus implementing a current reference source of 30 μA.



(a) Start-up with CMOS Inverter (b) Start-up with MOS Capacitor

Fig. 7. Transient Simulation of I_1, I_2 and I_{ST} of start-up circuit.

The results showed that the halo-implanted transistors are not able to maintain the intended biasing and is more susceptible to temperature and supply voltage variations, because it does not have a well-defined saturation current and it presents high mismatch compared to uniformly doped transistors.

Thus, the best choice between these implementations is a current reference source built with uniformly doped transistors with a $S^{I_Q}_{V_{DD}}$ of 0.7% and a TC of 23.8 ppm/ºC. For the start-up circuit, the best option between the designs presented in this manuscript is the start-up with a MOS transistor operating as a capacitor, which presents the smaller current drain.

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